

What is claimed is:

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1. A method of creating a hybridized chip using a top active optical device, having a substrate including a first side and active device contacts on the first side, the top active optical device also being on the first side, combined with an electronic chip having electronic chip contacts, when at least some of the active device contacts are not aligned with at least some of the electronic chip contacts, each of the at least some active device contacts having an electrically corresponding electronic chip contact, the method comprising:

creating sidewalls defining openings in the substrate, extending from the first side at the active device contacts to a bottom of the substrate opposite the first side, at points substantially coincident with the active device contacts;

making the sidewalls electrically conductive; and

connecting the points and the electronic chip contacts with an electrically conductive material.

2. The method of claim 1 wherein the making the sidewalls electrically conductive comprises:

filling at least some of the openings with an electrically conductive material.

3. The method of claim 1 wherein the making the sidewalls electrically conductive comprises:

depositing an electrically conductive material on at least some of the sidewalls.

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4. The method of claim 1 further comprising:
attaching a carrier to the top active optical device.

5. The method of claim 4 further comprising:
removing the carrier after connecting the points and the electronic chip contacts.

6. The method of claim 1 wherein the connecting comprises:
patterning traces between the points and the electronic chip contacts, and
making the traces electrically conductive.

7. The method of claim 6 wherein the patterning traces comprises:
patterning the traces on the substrate.

8. The method of claim 6 wherein the patterning traces comprises:
patterning the traces on the electronic chip.

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9. The method of claim 1 further comprising:
thinning the substrate.
10. The method of claim 1 further comprising attaching a carrier having a thickness
greater than a minimum lasing thickness over the top active device.

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14. The method of claim 13 wherein the insulator has holes defined by sidewalls, and
 forming the electrically conductive paths comprises:

of claim 14 wherein the

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filling the holes with an electrically conductive material.

16. The method of claim 14 wherein the making the holes electrically conductive comprises:

depositing an electrically conductive material on the sidewalls.

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17. The method of claim 13, wherein the insulator is part of one of the two chips, the method further comprising:

joining the other of the two chips to the insulator.

18. The method of claim 13, wherein the insulator is part of neither of the two chips, the method further comprising:

joining both of the two chips to the insulator.

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19. A module comprising:

two chips connected together according to the method of one of claims 13-18

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